CLAIMS

I/We claim:

[c1] 1. An active pixel comprising:

a light sensing element formed in a semiconductor substrate;

a transfer gate adjacent to said light sensing element for transferring out a signal from said light sensing element;

a memory gate adjacent to said transfer gate;

a control gate adjacent to said memory gate for transferring out said signal to a sense node; and

an amplification transistor controlled by said sense node.

[c2] 2. The pixel of Claim 1 wherein said light sensing element is selected from the group of photodiode, pinned photodiode, partially pinned photodiode, or photogate.

[c3] 3. The pixel of Claim 1 wherein said memory gate when activated forms a memory well in said substrate underneath said memory gate, said memory well capable of storing said signal from said light sensing element.

[c4] 4. The pixel of Claim 1 wherein said amplification transistor outputs an amplified version of said signal to a column bitline.

[c5] 5. The pixel of Claim 1 further including a reset transistor operative to reset said sense node to a reference voltage.

[c6] 6. An active pixel comprising:

a photodiode formed in a semiconductor substrate;

a transfer gate adjacent to said light sensing element for transferring out a signal from said light sensing element;

a memory gate adjacent to said transfer gate;

a control gate adjacent to said memory gate for transferring out said signal to a sense node;

an amplification transistor controlled by said sense node, wherein said amplification transistor outputs an amplified version of said signal to a column bitline;

a reset transistor operative to reset said sense node to a reference voltage.

[c7] 7. An apparatus comprising:

a first pixel comprising:

a first light sensing element formed in a semiconductor substrate;

a first transfer gate adjacent to said first light sensing element for transferring out a first signal from said first light sensing element;

a first memory gate adjacent to said first transfer gate;

a first control gate adjacent to said first memory gate for transferring out said first signal to a sense node;

a second pixel comprising:

a second light sensing element formed in a semiconductor substrate;

a second transfer gate adjacent to said second light sensing element for transferring out a second signal from said second light sensing element;

a second memory gate adjacent to said second transfer gate;

a second control gate adjacent to said second memory gate for transferring out said second signal to a sense node;

a reset transistor coupled to the output node for resetting the output node to a reference voltage; and

an output transistor that is coupled to the sense node.

[c8] 8. The apparatus of Claim 7 wherein said first pixel is in a first row of an imaging array and said second pixel is in a second row of an image array adjacent to said first row.

[c9] 9. The apparatus of Claim 7, wherein the output transistor is connected to a column bitline without the use of a row select transistor.

[c10] 10. The apparatus of Claim 7, wherein said output transistor has its gate coupled to said output node.

[c11] 11. An active pixel comprising:

a light sensing element formed in a semiconductor substrate;

a transfer gate adjacent to said light sensing element for transferring out a signal from said light sensing element;

a first memory gate adjacent to said transfer gate;

a second memory gate adjacent to said first memory gate;

a control gate adjacent to said second memory gate for transferring out said signal to a sense node; and

an amplification transistor controlled by said sense node.

[c12] 12. The pixel of Claim 11 wherein said light sensing element is selected from the group of photodiode, pinned photodiode, partially pinned photodiode, or photogate.

[c13] 13. The pixel of Claim 11 wherein when either of said memory gates are activated forms a memory well in said substrate underneath the respective said memory gate, said memory well capable of storing said signal from said light sensing element.

[c14] 14. The pixel of Claim 11 wherein said first and second memory gates are selectively activated to alternately store said signal from said light sensing element.

[c15] 15. The pixel of Claim 14 wherein said first and second memory gates operate at a frequency of greater than 1000 Hertz.

[c16] 16. The pixel of Claim 11 wherein said first and second memory gates, said transfer gate, and said control gate are formed from the same layer of polysilicon.

[c17] 17. The pixel of Claim 11 further including a reset transistor operative to reset said sense node to a reference voltage.

[c18] 18. An active pixel comprising:

a light sensing element formed in a semiconductor substrate;

a transfer gate adjacent to said light sensing element for transferring out a signal from said light sensing element;

a memory gate adjacent to said transfer gate;

a p-type layer formed in the surface of said semiconductor substrate underneath said memory gate;

a control gate adjacent to said memory gate for transferring out said signal to a sense node; and

an amplification transistor controlled by said sense node.

[c19] 19. The pixel of Claim 18 wherein said light sensing element is selected from the group of photodiode, pinned photodiode, partially pinned photodiode, or photogate.

[c20] 20. The pixel of Claim 18 wherein said memory gate when activated forms a memory well in said substrate underneath said memory gate, said memory well capable of storing said signal from said light sensing element.

[c21] 21. The pixel of Claim 18 further including an n-channel formed in said semiconductor substrate and beneath said p-type layer.

[c22] 22. The pixel of Claim 18 further including a second control gate between said control gate and said sense node.

[c23] 23. The pixel of Claim 18 further including a reset transistor operative to reset said sense node to a reference voltage.